

CLAIMS

1 1. In a data processing system having a first component and a second
2 component, wherein said first component, the improvement comprising:

3 a. A first data bus having a first set of characteristics responsively
4 coupled between said first component and said second component;

5 b. A second data base having a second set of characteristics
6 responsively coupled between said first component and said second
7 component; and

8 c. A circuit responsively coupled to said first data bus and said second
9 data bus which combines said first data bus and said second data bus into a
10 logical bus having a third set of characteristics wherein said third set of
11 characteristics is different from either said first set of characteristics and said
12 second set of characteristics.

1 2. A data processing system according to claim 1 wherein said first set of
2 characteristics includes a first maximum transfer rate, said second set of
3 characteristics includes a second maximum transfer rate, and said third set of
4 characteristics includes a third maximum transfer rate and wherein said third
5 maximum transfer rate is greater than either of said first maximum transfer rate and
6 said second maximum transfer rate.

1 3. A data processing system according to claim 2 wherein said third maximum
2 transfer rate is the sum of said first maximum transfer rate and said second maximum
3 transfer rate.

1 4. A data processing system according to claim 3 wherein said first maximum
2 transfer rate and said second maximum transfer rate are equal.

1 5. A data processing system according to claim 4 wherein said first maximum
2 transfer rate is equal to 33MHz.

1 6. A data processing system comprising:

2 a. A first component;

3 b. A second component;

4 c. A first data bus responsively coupled between said first component
5 and said second component;

6 d. A second data bus responsively coupled between said first
7 component and said second component; and

8 e. A circuit responsively coupled to said first data bus and said second
9 data bus which combines said first data bus and said second data bus into a
10 logical bus.

1 7. A data processing system according to claim 6 wherein said first data bus
2 has a first set of characteristics, said second data bus has a second set of
3 characteristics, said logical bus has a third set of characteristics, and said third set of
4 characteristics is different from said first set of characteristics and said second set of
5 characteristics.

1 8. A data processing system according to claim 7 wherein said first set of
2 characteristics includes a first data transfer rate, said second set of characteristics
3 includes a second data transfer rate, said third set of characteristics includes a third
4 data transfer rate, and said third data transfer rate is greater than either of said first
5 data transfer rate and said second data transfer rate.

1 9. A data processing system according to claim 8 wherein said third data
2 transfer rate equals the sum of said first data transfer rate and said second data
3 transfer rate.

1 10. A data processing system according to claim 9 wherein said first data
2 transfer rate is equal to said second data transfer rate.

1 11. A method of coupling a first component to a second component within a
2 data processing system comprising:

3 a. Providing a first data bus having a first set of characteristics
4 responsively coupled between said first component and said second
5 component;

6 b. Providing a second data bus having a second set of characteristics
7 responsively coupled between said first component and said second
8 component; and

9 c. Combining said first data bus and said second data bus to produce a
10 logical bus having a third set of characteristics'

1 12. A method according to claim 11 wherein said first set of characteristics
2 includes a first data transfer rate, said second set of characteristics includes a second
3 data transfer rate, said third set of characteristics includes a third data transfer rate,
4 and said third data transfer rate is greater than either of said first data transfer rate
5 and said second data transfer rate.

1 13. A method according to claim 12 wherein said third data transfer rate is
2 equal to the sum of said first data transfer rate and said second data transfer rate.

1 14. A method according to claim 13 wherein said first data transfer rate is
2 equal to said second data transfer rate.

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1 15. A method according to claim 14 wherein said first data transfer rate is
2 equal to 33MHz.

1 16. An apparatus comprising:

2 a. First means for performing a first data processing function;

3 b. Second means for performing a second data processing function;

4 c. First means responsively coupled to said first performing means and
5 said second performing means for transferring data from said first performing
6 means to said second performing means in accordance with a first set of
7 characteristics;

8 d. Second means responsively coupled to said first performing means
9 and said second performing means for transferring data from said first
10 performing means to said second performing means in accordance with a
11 second set of characteristics; and

12 e. Means responsively coupled to said first transferring means and said
13 second transferring means for combining said first transferring means and
14 said second transferring means into a logical transferring means having a third
15 set of characteristics.

1 17. An apparatus according to claim 16 wherein said first set of characteristics
2 includes a first transfer rate, said second set of characteristics includes a second
3 transfer rate, said third set of characteristics includes a third transfer rate, and said

4 third transfer rate is greater than either of said first transfer rate and said second
5 transfer rate.

1 18. An apparatus according to claim 17 wherein said third transfer rate equals
2 the sum of said first transfer rate and said second transfer rate.

1 19. An apparatus according to claim 18 wherein said first transfer rate equals
2 said second transfer rate.

1 20. An apparatus according to claim 19 wherein said first transfer rate is equal
2 to 33MHz.

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